REMARKS

Claim Rejections Under 35 U.S.C. § 102

Claims 1, 3, 4, 6, 11, 13-17, 19 -21 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Yuan et al.* (U.S. Patent No. 6,762,092 B2). Applicant respectfully traverses this rejection.

Claim 1 has been amended to correct a typographical error in the first element. The trenches are formed between pairs of oxide pillars and not between "each oxide pillar" as originally stated.

Yuan et al. discloses a scalable, self-aligned dual floating gate memory cell array. The Examiner alleges that Figure 25A of *Yuan et al.* shows the plurality of oxide pillars as claimed by Applicant. Since the Examiner has not specifically indicated the oxide pillars in *Yuan et al.*, Applicant assumes the oxide pillars to which the Examiner refers are spacers 407 that are composed of "a thick layer of oxide over the structure" (column 16, lines 18 – 19). However, these spacers 407, nor any other pillar-like structures of *Yuan et al.*, do not each have a source/drain region as claimed in the present claims. The source and drain regions 449, 451 of *Yuan et al.* are implanted in the substrate 445 as shown in Figure 25A and discussed at col. 16, lines 20 – 24.

The Examiner further states that *Yuan et al.'s* dielectric layers 406 are analogous to Applicant's gate insulator layers that have a structure for trapping at least one charge. However, the only dielectric layers 406 (Examiner's gate insulator layers) that are located between strips 410, 412 (Examiner's program gates) and the spacers 407 (Examiner's oxide pillars), are also outside of any channel region that may be created by the source and drain regions 449, 451. Yuan et al. does not teach or suggest that these dielectric layers 406 are used for trapping a charge. In fact, it is highly unlikely that these dielectric layers 406 have a capability for storing a charge since neither channel hot electron injection nor source side injection can cause injection of electrons to these dielectric layers 406 outside of the channel region. *Yuan et al.*, therefore, neither teaches nor suggests Applicant's invention as claimed.

Claim Rejections Under 35 U.S.C. § 103

Claims 8-10, 12 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yuan et al.* (U.S. Patent No. 6,762,092) in view of *Chien et al.* (U.S. Patent No. 6,069,042). Applicant respectfully traverses this rejection.

Chien et al. discloses a flash EEPROM device that has an interpoly dielectric composed of an ONO composite film. However, *Chien et al.* neither teaches nor suggests Applicant's invention as claimed. Additionally, for the above-discussed reasons, even if it were obvious to combine *Chien et al.* with *Yuan et al.*, the combination cannot produce Applicant's claimed invention.

Allowable Subject Matter

Claims 2, 5, 7 and 22-25 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims.

CONCLUSION

For the foregoing reasons, Applicant believes the present invention is in condition for allowance. Therefore, Applicant respectfully requests withdrawal of the rejection and allowance of claims 1 – 25. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No additional matter has been entered and no additional fee is required by this amendment and response.

Respectfully submitted,

Date: 11/12/04

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